IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising an MIM structure capacitor connected between a power source potential electrode wiring and a ground potential electrode wiring each via at least one interlayer connection wiring[.], wherein said power source potential electrode wiring comprises a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring comprises a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

Claim 2 (Original): The semiconductor integrated circuit device according to claim 1, wherein a metal electrode on one side of said MIM structure capacitor is connected to said power source potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

Claim 3 (Original): The semiconductor integrated circuit device according to claim 2, wherein a metal electrode on the other side of said MIM structure capacitor is connected to said ground potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

Claim 4 (Original). The semiconductor integrated circuit device according to claim 1, wherein said power source potential electrode wiring and said ground potential electrode wiring are adjacent to each other via an insulation film.

Claim 5-6 (Cancelled) .

Claim 7 (Currently Amended). A semiconductor integrated circuit device comprising:

a metal electrode on one side of an MIM structure capacitor connected to a power source potential electrode wiring via at least one interlayer connection wiring;

a metal electrode on the other side of the MIM structure capacitor connected to a ground potential electrode wiring via at least one interlayer connection wiring; and

an insulation dielectric sandwiched by said metal electrode on one side of the MIM structure capacitor and said metal electrode on the other side[.] of the MIM structure capacitor,

wherein said power source potential electrode wiring comprises a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring comprises a loop-shape ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

Claim 8 (Original): The semiconductor integrated circuit device according to claim 7, wherein said metal electrode on one side is connected to said power source potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

Claim 9 (Original): The semiconductor integrated circuit device according to claim 7, wherein said metal electrode on the other side is connected to said ground potential electrode wiring via two or more interlayer connection wirings and at least one metal wiring layer.

Claim 10 (Original): The semiconductor integrated circuit device according to claim 7, wherein said power source potential electrode wiring and said ground potential electrode wiring are adjacent to each other via an insulation film.

Claim 11-12 (Cancelled).

Claims 13 (Withdrawn): A method of manufacturing a semiconductor integrated circuit device comprising:

forming an MIM structure capacitor;

covering said MIM structure capacitor with an interlayer insulation film;

opening contact holes in said interlayer insulation film on a metal electrode on one side and a metal electrode on the other side of said MIM structure capacitor;

forming an interlayer connection wiring in said contact holes; and

forming a power source potential electrode wiring and a ground potential electrode wiring connected to said metal electrode on one side and said metal electrode on the other side, respectively, each via said interlayer connection wiring.

Claim 14 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 13, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said power source potential electrode wiring and said metal electrode on one side.

Claim 15 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 13, further forming two or more interlayer connection

wirings including said interlayer connection wiring a»d at least one metal wiring layer between said ground potential electrode wiring and said metal electrode on the other side.

Claim 16 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said power source potential electrode wiring and said ground potential electrode wiring are formed so as to be adjacent to each other via an insulation film.

Claim 17 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said power source potential electrode wiring is formed as a power source potential electrode pad to which a power source potential is supplied and an external wiring is connected, and said ground potential electrode wiring is formed as a ground potential electrode pad which is grounded and to which an external wiring is connected.

Claim 18 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 13, where said power source potential electrode wiring is formed as a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring is formed as a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.

Claim 19 (Withdrawn): A method of manufacturing a semiconductor integrated circuit device comprising:

forming a metal electrode on one side;

forming an insulation dielectric on a part of said metal electrode on one side;

forming a metal electrode on the other side on said insulation dielectric;

covering said metal electrode on one side, said metal electrode on the other side, and said insulation dielectric with an interlayer insulation film;

opening contact holes in said interlayer insulation film on said metal electrode on one side and said metal electrode on the other side;

forming an interlayer connection wiring in said contact holes; and

forming a power source potential electrode wiring and a ground potential electrode wiring connected to said metal electrode on one side and said metal electrode on the other side, respectively, each via said interlayer connection wiring.

Claim 20 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 19, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said power source potential electrode wiring and said metal electrode on one side.

Claim 21 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 19, further forming two or more interlayer connection wirings including said interlayer connection wiring and at least one metal wiring layer between said ground potential electrode wiring and said metal electrode on the other side.

Claim 22 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring

and said ground potential electrode wiring are formed so as to be adjacent to each other via an insulation film.

Claim 23 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring is formed as a power source potential electrode pad to which a power source potential is supplied and

an external wiring is connected, and said ground potential electrode wiring is formed as a ground potential electrode pad which is grounded and to which an external wiring is connected.

Claim 24 (Withdrawn): The method of manufacturing a semiconductor integrated circuit device according to claim 19, wherein said power source potential electrode wiring is formed as a loop-shaped power source potential electrode wiring which is formed in a loop shape around a semiconductor integrated circuit body and to which a power source potential is supplied, and said ground potential electrode wiring is formed as a loop-shaped ground potential electrode wiring which is formed in a loop shape around the semiconductor integrated circuit body and is grounded.